UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/529,880	11/17/2005	Yoshifumi Yaoi	0020-5364PUS1	7737

2292 7590 06/15/2007

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
TRAN, MICHAEL THANH	

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
06/15/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/529,880	YAOI ET AL.	
	Examiner	Art Unit	
	MICHAEL T. TRAN	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *April 1, 2005 through November 2, 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34,45,47-51 and 53-76* is/are rejected.

7)☒ Claim(s) *35-44,46 and 52* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MICHAEL TRAN
AU 2827

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/1/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the Communications dated April 1, 2005 through November 2, 2006, claims 34-76 are active in this application as a result of the cancellation of claims 1-33.

Foreign Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a) (d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statements filed April 1, 2005 have been considered.

Claim Objections

4. Claims 35-44, 46 and 52 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

It appears that the word "a", first occurrence, 3rd line, of claims 66 and 67 should be deleted.

Claim Rejections- 35 U.S.C. § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claim 47 is rejected under 35 U.S.C 102(b) as being anticipated by Koga et al. [U.S. Patent # 6,683,491].

With respect to claim 47, Koga et al. disclose, in figure 3, a semiconductor storage device comprising: power supply switches [16 and 18] that stop supplying at least one of a plurality of power voltages supplied from outside when a memory circuit including a memory cell array is in a standby state; and a lockout circuit that inhibits a command to the memory circuit when ally one of the plurality of power voltages is lower than a prescribed voltage. See the entire document, especially, the "Detailed Description" section.

5. Claim 48 is rejected under 35 U.S.C 102(b) as being anticipated by Koga et al. [U.S. Patent # 6,683,491].

With respect to claim 48, Koga et al. disclose, in figure 3, A semiconductor storage device control method for inhibiting a command to a memory circuit including a

memory cell array, comprising the steps of: stopping supply of at least one of a plurality of power voltages supplied from outside when the memory circuit is in a standby state; and inhibiting the command to the memory circuit when any one of the plurality of power voltages is lower than a prescribed voltage. See the entire document, especially, the "Detailed Description" section.

6. Claims 49-51 and 53-60 are rejected under 35 U.S.C 102(b) as being anticipated by Koga et al. [U.S. Patent # 6,683,491].

With respect to claim 49, Koga et al. disclose, in figure 3, A semiconductor storage device control method for inhibiting a command to a memory circuit including a memory cell array, comprising the steps of [See figure 6]: investigating whether or not the memory circuit is in a standby state; stopping supply of the power voltage to the memory circuit and inhibiting the command to the memory circuit when the memory circuit is in the standby state; confirming at least one of the plurality of power voltages by a power voltage confirmation circuit; and outputting a lockout signal for inhibiting the command from the power voltage confirmation circuit to the memory circuit when any one of the plurality of power voltages is lower than a prescribed voltage. See the entire document, especially, the "Detailed Description" section.

With respect to claim 50, Koga et al. disclose, in figure 3, the command is a rewrite command. Koga et al. indicated that all functions stop operation during a sleep mode. See the entire document, especially, the "Detailed Description" section.

With respect to claim 51, Koga et al. disclose, in figure 3, at least one of the plurality of power voltages is compared with the prescribed voltage by a comparator. See the entire document, especially, the "Detailed Description" section.

With respect to claim 53, Koga et al. disclose, in figure 3, a voltage detector detects whether or not a first power voltage supplied to the memory circuit including the memory cell array among the plurality of power voltages is outside a predetermined range, and a lockout signal for inhibiting the command to tile memory circuit is outputted from the voltage detector when tile first power voltage is outside the predetermined range. See the entire document, especially, the "Detailed Description" section.

With respect to claim 54, Koga et al. disclose, in figure 3, the command to the memory circuit including the memory cell array is inhibited when at least one of the lockout signal from the voltage detector and the lockout signal from the power voltage confirmation circuit is outputted. See the entire document, especially, the "Detailed Description" section.

With respect to claim 55, Koga et al. disclose, in figure 3, the supply state of a power voltage of the voltage detector is controlled by the first power voltage. See the entire document, especially, the "Detailed Description" section.

With respect to claim 56, Koga et al. disclose, in figure 3, the lockout signal for inhibiting the command to the memory circuit is outputted from the power voltage confirmation circuit when the power voltage supplied to the output circuit among the plurality of power voltages is lower than the prescribed voltage. See the entire document, especially, the "Detailed Description" section.

With respect to claim 57, Koga et al. disclose, in figure 3, the plurality of power voltages are confirmed by the power voltage confirmation circuit. See the entire document, especially, the "Detailed Description" section.

With respect to claim 58, Koga et al. disclose, in figure 3, the command to the memory circuit including the memory cell array is inhibited on the basis of at least one of the plurality of power voltages. See the entire document, especially, the "Detailed Description" section.

With respect to a claim 59, Koga et al. disclose, in figure 3, tile lockout signal for inhibiting the command to tile memory circuit is outputted from the power voltage confirmation circuit when the power voltage supplied to the memory circuit including the memory cell array among the plurality of power voltages is outside predetermined range. See the entire document, especially, the "Detailed Description" section.

With respect to a claim 60, Koga et al. disclose, in figure 3, the prescribed voltage for determining the power voltage supplied to the output circuit among the plurality of power voltages is within a range of O.3 V to 1.2 V. See the entire document, especially, the "Detailed Description" section. Further, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Claim Rejections - 35 U.S.C. § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 34, 63, 66, and 69 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Miyatake et al. [U.S. Patent # 5,963,467] in view of Mizutani [U.S. Patent # 4,882,707].

Miyatake et al. disclose a semiconductor storage device comprising: a memory cell array employing a memory element [inherent feature – figure 14 shows one memory cell as a simplified representation of an overall circuit] as a memory cell wherein the memory element is constructed of a gate electrode formed via a gate insulation film on a semiconductor layer, a channel region arranged under the gate electrode, diffusion regions that are arranged on both sides of the channel region and have a conductive type opposite to that of the channel region and memory function bodies that are formed on both sides of the gate electrode and have a function to retain electric charges [see figure 9 – inherent, but since Miyatake et al. is silent about various description of the structural limitations, another reference is brought in to clarify the inherency features]; and a lockout circuit [Power on monitor circuit] that inhibits a command to a memory circuit including the memory cell array when a power voltage supplied from outside is lower than a prescribed voltage [see abstract and the "Summary of the Invention" sections].

Miyatake et al. disclose all of the above mentioned but is silent about the structural limitations of the claimed memory cell. However, this is not new. Mizutani disclose all claimed features of the memory cell. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Miyatake et al. memory device to include the memory cell as taught by Mizutani, since the modification is merely a substitution of a functionally recognized equivalent element. See the entire patent, specifically the "Summary of the Invention" section.

With respect to claim 63, Miyatake et al. disclose, in figure 9, at least part of the memory function bodies possessed by the memory element overlaps with part of a diffusion region. Also see Mizutani, if the details of the memory structure are not as clear.

With respect to claim 66, Miyatake et al. disclose, in figure 9, there is provided an insulation film [any in the surrounding of the channel] for isolating from the channel region or the semiconductor layer [a] film [any of the surrounding layer of the channel] which has a surface roughly parallel to a surface of the gate insulation film of the memory element and has a function to retain electric charges, and a film thickness of the insulation film is thinner than a film thickness of the gate insulation film and is not smaller than 0.8 nm. Also see Mizutani, if the details of the memory structure are not as clear. Further, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

With respect to claim 69, Miyatake et al. disclose, in figure 9, the memory function bodies possessed by the memory element comprise a film that has a surface roughly parallel to a surface of the gate insulation film and has a function to retain electric charges. Also see Mizutani, if the details of the memory structure are not as clear.

9. Claim 45 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Miyatake et al. [U.S. Patent # 5,963,467] in view of Mizutani [U.S. Patent # 4,882,707] and Hsu et al. [U.S. Patent # 6,343,044].

Miyatake et al. disclose a semiconductor storage device comprising: a memory cell array employing a memory element [inherent feature – figure 14 shows one memory cell as a simplified representation of an overall circuit] as a memory cell wherein the memory element is constructed of a gate electrode formed via a gate insulation film on a semiconductor layer, a channel region arranged under the gate electrode, diffusion regions that are arranged on both sides of the channel region and have a conductive type opposite to that of the channel region and memory function bodies that are formed on both sides of the gate electrode and have a function to retain electric charges [see figure 9 – inherent, but since Miyatake et al. is silent about various description of the structural limitations, another reference is brought in to clarify the inherency features]; and a lockout circuit [Power on monitor circuit] that inhibits a command to a memory circuit including the memory cell array when a power voltage supplied from outside is

lower than a prescribed voltage [see abstract and the "Summary of the Invention" sections].

Miyatake et al. disclose all of the above mentioned but is silent about the structural limitations of the claimed memory cell and the application of power switches for controlling power during active and inactive modes. However, these are not new. Mizutani disclose all claimed features of the memory cell [See the entire patent, specifically the "Summary of the Invention" section], and Hsu et al., disclose the application of switching elements for use during an active/inactive modes [figure 3a – 50]. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Miyatake et al. memory device to include the memory cell as taught by Mizutani, since the modification is merely a substitution of a functionally recognized equivalent element. Further, it would also have been obvious to add the power switching elements, as taught by Hsu et al., into the memory device of Miyatake et al. since it would enhance the memory device by reducing the power consumption.

10. Claims 61, 62, 65, 68, 71 and 74 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Miyatake et al. [U.S. Patent # 5,963,467] in view of Mizutani [U.S. Patent # 4,882,707] and Hsu et al. [U.S. Patent # 6,343,044].

Miyatake et al. disclose A semiconductor storage device comprising: a memory cell array employing a memory element as a memory cell wherein the memory element [inherent feature – figure 14 shows one memory cell as a simplified representation of an

overall circuit] is constructed of a gate electrode formed via a gate insulation film on a semiconductor layer, a channel region arranged under the gate electrode, diffusion regions that are arranged on both sides of the channel region and have a conductive type opposite to that of the channel region and memory function bodies that are formed on both sides of the gate electrode and have a function to retain electric charges [see figure 9 – inherent, but since Miyatake et al. is silent about various description of the structural limitations, another reference is brought in to clarify the inherency features]; and power supply [see figure 14] is turned on to supply the power voltage to at least the memory circuit including the memory cell array when the memory circuit is in an active state and is turned off to stop the supply of the power voltage to at least the memory circuit including the memory cell array when the memory circuit is in a standby state.

Miyatake et al. disclose all of the above mentioned but is silent about the structural limitations of the claimed memory cell and the application of power switches for controlling power during active and inactive modes. However, these are not new. Mizutani disclose all claimed features of the memory cell [See the entire patent, specifically the "Summary of the Invention" section], and Hsu et al., disclose the application of switching elements for use during an active/inactive modes [figure 3a – 50]. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Miyatake et al. memory device to include the memory cell as taught by Mizutani, since the modification is merely a substitution of a functionally recognized equivalent element. Further, it would also have been obvious to add the power switching elements, as taught by Hsu et al., into the memory device of

Miyatake et al. since it would enhance the memory device by reducing the power consumption.

With respect to claim 62, both Hsu et al. and Miyatake et al. disclose, the power supply switches are formed on a substrate identical to that of the memory circuitincluding the memory cell array.

With respect to claim 65, Miyatake et al. and Mizutani disclose at least part of the memory function bodies possessed by the memory element overlaps with part of a diffusion region.

With respect to claim 68, Mizutani disclose, that there is provided an insulation film [any surrounding the channel region] for isolating from the channel region or the semiconductor layer [a] film [any surrounding the gate] which has a surface roughly parallel to a surface of the gate insulation film of the memory element and has a function to retain electric charges, and a film thickness of the insulation film is thinner than a film thickness of the gate insulation film and is not smaller than 0.8 nm [See the entire patent, specifically the "Summary of the Invention" section]. Further, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

With respect to claim 71, Mizutani disclose, that the memory function bodies possessed by the memory element comprise a fihn that has a surface roughly parallel to a surface of the gate insulation film and has a function to retain electric charges [See the entire patent, specifically the "Summary of the Invention" section].

With respect to claim 74, it has been held that making an old device portable or movable without producing any new and unexpected result involves only routine skill in the art. In re Lindberg, 93 USPQ 23 [CCPA 1952].

11. Claim 64 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Koga et al. [U.S. Patent # 6,683,491] in view of Mizutani [U.S. Patent # 4,882,707].

Koga et al. disclose, in figure 3, a semiconductor storage device comprising: power supply switches [16 and 18] that stop supplying at least one of a plurality of power voltages supplied from outside when a memory circuit including a memory cell array is in a standby state; and a lockout circuit that inhibits a command to the memory circuit when ally one of the plurality of power voltages is lower than a prescribed voltage. See the entire document, especially, the "Detailed Description" section.

Koga et al. disclose all of the above mentioned but is silent about the structural limitations of the claimed memory cell, specifically, at least part of the memory function bodies possessed by the memory element overlaps with part of a diffusion region. However, these are not new. Mizutani disclose all claimed features of the memory cell [See the entire patent, specifically the "Summary of the Invention" section]. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Koga et al. memory device to include the memory cell as taught by Mizutani, since the modification is merely a substitution of a functionally recognized equivalent element.

With respect to claim 67, Mizutani disclose, that there is provided an insulation film [any surrounding the channel region] for isolating from the channel region or the semiconductor layer [a] film [any surrounding the gate] which has a surface roughly parallel to a surface of the gate insulation film of the memory element and has a function to retain electric charges, and a film thickness of the insulation film is thinner than a film thickness of the gate insulation film and is not smaller than 0.8 nm [See the entire patent, specifically the "Summary of the Invention" section]. Further, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

With respect to claim 70, Mizutani disclose, that the memory function bodies possessed by the memory element comprise a fihn that has a surface roughly parallel to a surface of the gate insulation film and has a function to retain electric charges [See the entire patent, specifically the "Summary of the Invention" section].

12. Claim 72 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Miyatake et al. [U.S. Patent # 5,963,467] in view of Mizutani [U.S. Patent # 4,882,707] and Kumanoya et al [U.S. Patent #4,933,907].

Miyatake et al. disclose a semiconductor storage device comprising: a memory cell array employing a memory element [inherent feature – figure 14 shows one memory cell as a simplified representation of an overall circuit] as a memory cell wherein the memory element is constructed of a gate electrode formed via a gate insulation film on

a semiconductor layer, a channel region arranged under the gate electrode, diffusion regions that are arranged on both sides of the channel region and have a conductive type opposite to that of the channel region and memory function bodies that are formed on both sides of the gate electrode and have a function to retain electric charges [see figure 9 – inherent, but since Miyatake et al. is silent about various description of the structural limitations, another reference is brought in to clarify the inherency features]; and a lockout circuit [Power on monitor circuit] that inhibits a command to a memory circuit including the memory cell array when a power voltage supplied from outside is lower than a prescribed voltage [see abstract and the "Summary of the Invention" sections].

Miyatake et al. disclose all of the above mentioned but is silent about the structural limitations of the claimed memory cell as well as the application of the memory device within a portable device. However, these are not new. Mizutani disclose all claimed features of the memory cell [See the entire patent, specifically the "Summary of the Invention" section]. Kumanoya et al. disclose the application of a memory device such as dram within a portable device. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Miyatake et al. memory device to include the memory cell as taught by Mizutani, since the modification is merely a substitution of a functionally recognized equivalent element. Further, Kumanoya et al. indicated that it is necessary for a portable device to have a memory element such as drams to store information. Furthermore, it has been held that making an old device portable or movable without

producing any new and unexpected result involves only routine skill in the art. In re Lindberg, 93 USPQ 23 [CCPA 1952].

13. Claim 73 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Koga et al. [U.S. Patent # 6,683,491] in view of Kumanoya et al [U.S. Patent #4,933,907].

Koga et al. disclose, in figure 3, a semiconductor storage device comprising: power supply switches [16 and 18] that stop supplying at least one of a plurality of power voltages supplied from outside when a memory circuit including a memory cell array is in a standby state; and a lockout circuit that inhibits a command to the memory circuit when ally one of the plurality of power voltages is lower than a prescribed voltage. See the entire document, especially, the "Detailed Description" section.

Koga et al. disclose all of the above mentioned but is silent about the application of the memory device within a portable medium. However, this is not new. Kumanoya et al. disclose that application of memory devices such as dram within portable computers is a necessity. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Koga et al. memory device to include the memory cell as taught by Kumanoya et al., since the modification is merely a substitution of a functionally recognized equivalent element. Further, without memory devices, there would not be a way to store data. Furthermore, it has been held that making an old device portable or movable without producing any

new and unexpected result involves only routine skill in the art. In re Lindberg, 93 USPQ 23 [CCPA 1952].

14. Claim 75 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Koga et al. [U.S. Patent # 6,683,491] in view of Kumanoya et al [U.S. Patent #4,933,907].

Koga et al. disclose, in figure 3, a semiconductor storage device comprising: power supply switches [16 and 18] that stop supplying at least one of a plurality of power voltages supplied from outside when a memory circuit including a memory cell array is in a standby state; and a lockout circuit that inhibits a command to the memory circuit when ally one of the plurality of power voltages is lower than a prescribed voltage. See the entire document, especially, the "Detailed Description" section.

Koga et al. disclose all of the above mentioned but is silent about the application of the memory device within a portable medium. However, this is not new. Kumanoya et al. disclose that application of memory devices such as dram within portable computers is a necessity. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Koga et al. memory device to include the memory cell as taught by Kumanoya et al., since the modification is merely a substitution of a functionally recognized equivalent element. Further, without memory devices, there would not be a way to store data. Furthermore, it has been held that making an old device portable or movable without producing any

new and unexpected result involves only routine skill in the art. In re Lindberg, 93 USPQ 23 [CCPA 1952].

15. Claim 76 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Koga et al. [U.S. Patent # 6,683,491] in view of Kumanoya et al [U.S. Patent #4,933,907].

Koga et al. disclose, in figure 3, A semiconductor storage device control method for inhibiting a command to a memory circuit including a memory cell array, comprising the steps of [See figure 6]: investigating whether or not the memory circuit is in a standby state; stopping supply of the power voltage to the memory circuit and inhibiting the command to the memory circuit when the memory circuit is in the standby state; confirming at least one of the plurality of power voltages by a power voltage confirmation circuit; and outputting a lockout signal for inhibiting the command from the power voltage confirmation circuit to the memory circuit when any one of the plurality of power voltages is lower than a prescribed voltage. See the entire document, especially, the "Detailed Description" section.

Koga et al. disclose all of the above mentioned but is silent about the application of the memory device within a portable medium. However, this is not new. Kumanoya et al. disclose that application of memory devices such as dram within portable computers is a necessity. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Koga et al. memory device to include the memory cell as taught by Kumanoya et al., since the modification is merely

a substitution of a functionally recognized equivalent element. Further, without memory devices, there would not be a way to store data. Furthermore, it has been held that making an old device portable or movable without producing any new and unexpected result involves only routine skill in the art. In re Lindberg, 93 USPQ 23 [CCPA 1952].

Allowable Subject Matter

16. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- the power voltage supplied from the outside is comprised of at least a first power voltage supplied to the memory circuit including the memory cell array and a second power voltage supplied to an output circuit (35), and the lockout circuit comprises: a voltage detector that outputs a first lockout signal for inhabiting the command to the memory circuit including the memory cell array when tile first power voltage is not higher than a first prescribed voltage; and a power voltage confirmation circuit that outputs a second lockout signal for inhibiting the command to the memory circuit including the memory cell array when the second power voltage is lower than a second prescribed voltage.

- supply states of power voltages of the comparator and a voltage generator circuit for generating the prescribed voltage are controlled by a first power voltage supplied to the memory circuit including the memory cell array among tile plurality of power voltages.

Conclusion

17. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

18..Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

19..Any inquiry of a general nature or relating to the status of this application. should be directed to the Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran
Art Unit 2827
June 9, 2007